New claims

1. A semi-conductor component, with a first pad and a second pad for receiving complementary clock signals (clk, bclk), and a clock receiver circuit device (1) for converting the received complementary clock signals (clk, bclk) into complementary clock output signals (clk, bclk) with different voltage levels as the received clock signals (clk, bclk), wherein the clock receiver circuit device (1) comprises a first clock input (9a) connected with the first pad, and a second clock input (8a) connected with the second pad,

wherein with a first and a third transfer gate (5, 6), a respective first transfer gate control connection is connected to the second clock input (8a) of the clock receiver circuit device (1), and a respective second transfer gate control connection inverse to the first control connection is connected to the first clock input (9a) of the clock receiver circuit device (1),

and wherein with a second and a fourth transfer gate (4, 7), a respective first transfer gate control connection is connected to the first clock input (9a) of the clock receiver circuit device (1), and a respective second transfer gate control connection inverse to the first control connection is connected to the second clock input (8a) of the clock receiver circuit device (1),

wherein a first further connection of the first transfer gate (5) is connected to a line (13), and a first further connection of the second transfer gate (4) is connected to a second line (12), and a first further connection of the third transfer gate (6) is connected to a third line (14), and a first further connection of the fourth transfer gate (7) is connected to a fourth line (15), to apply a first voltage to the first further connection of the first and fourth transfer gate, and a second voltage different therefrom to the first further connection of the second and third transfer gate,

wherein a second further connection of the first transfer gate (5) and a second further connection of the second transfer gate (4) are connected with one another, and are jointly connected to a first clock output (11b) to output a first clock output signal (bout), and a second further connection of the third transfer gate (6) and a second further connection of the fourth transfer gate (7) are connected with one

another, and are jointly connected to a second clock output (11a) to output a second clock output signal (out) complementary to the first clock output signal (bout).

2. The semi-conductor component of claim 1, additionally comprising a clock relaying circuit (2).

3. The semi-conductor component of claim 2, wherein the first clock output (11b) is connected to a first input of the clock relaying circuit (2), and the second clock output (11a) is connected to a second input of the clock relaying circuit (2).

4. The semi-conductor component of claim 9 or 3, wherein the clock relaying circuit (2) comprises four transistors (104a, 104b, 105a, 105b).